Performance Analysis of XOR/XNOR Circuits Using VTMOS and Reversible logic

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ABSTRACT: Power consumption, delay and area are the main considerations in VLSI systems. The prime motive of this work is to design a low power and high speed circuit with desired performance and diverse range of applications. The rapid growth of portable electronic devices emphasizes the need for energy and area efficient design to attract the end users. The exclusive OR (XOR) and exclusive NOR (XNOR) are the basic building blocks of many arithmetic and logic circuits like comparators, adders, linear shifters, crypto processors. The performance of the complex logic circuit is affected by the individual XOR/XNOR modules, therefore careful design is needed to obtain full voltage swing, less power consumption and delay. Here we focused on VTMOS logic for optimization. All circuits are simulated in HSPICE 130nm CMOS technology. The simulation results demonstrate that VTMOS exhibit less transistor count, decreased delay by 51.31%. Also compared reversible and irreversible logic for checking signal integrity. On an average, circuits with reversible logic exhibits 49.8 % improvement in delay and 48.3% improvement in PDP.

Keywords- VTMOS, optimization technique, reversible, irreversible.

1 INTRODUCTION

VLSI circuit is all about CMOS design. CMOS is simply the combination of PMOS and NMOS. The concept of more Moore results in more number of transistors gets integrated into a single IC chip. This led to the tremendous growth of VLSI industries. The International Technology Roadmap for Semiconductors (ITRS) helped to guide the industry by predicting the current technology trends and highlights the need for processing equipment requirements, industry standards, and market drivers [1]. The roadmap provides a paradigm for the semiconductor industry and helps to set the priorities for development and research. The concept to "More Moore" has successfully scaled Complementary Metal-Oxide Semiconductor (CMOS) devices and interconnects to achieve lower power, better speed, smaller size and higher outputs.

Fig 1. ITRS roadmap showing more Moore concept

In 1995, gate feature size was 250nm but today it has reached about 22nm. But dealing with the continuous scaling of horizontal and vertical feature size, short channel effects come into play. While considering the basic CMOS design the major scaling problems are static power dissipation, dynamic power dissipation and output signal degradation.

• Static power dissipation is due to leakage current. Leakage current is the main factor that degrades the performance of a circuit. Even for a small threshold voltage, circuit will be switched ON. This will affect the properties of the circuit. Static power dissipation occurs when all the inputs are at some logic level and the circuit is not in charging state. In a survey, they predicted that static power dissipation in 45nm technology will be 50% of the total power dissipation.

• Next is the dynamic power dissipation which results due to the charging and discharging of capacitors at the output. This also contributes to total power dissipation.

• At lower technology nodes, output signal degradation may occur and cannot sustain low voltage operation.
With the advent of portable electronic devices like laptops, cell phones etc there is an importance in considering a new cell design methodology for designing low power and high speed circuits and to incorporate less number of transistors. Normally we rely on creative design ideas to implement the logic but in this work we focused on different optimization and correction techniques like using transmission gates, bootstrap technique, feedback technique and variable thresholding technique. The main aim behind using these techniques is to reduce power consumption, delay and area. So if we are able to reduce the power, delay or area of a module in a circuit, we can ensure that the whole system will be energy and area efficient. Here we tried to reduce power, delay and area of XOR/XNOR circuits

2 XOR/XNOR CIRCUITS WITH OPTIMISATION TECHNIQUE

Technology scaling has expanded the transistor’s vulnerability to process variations in Very Large Scale Integrated (VLSI) Circuits especially in nanometer range [2]. The consequence of such variations will have a great impact on performance and hence affect the timing yield of the integrated circuits. The circuit optimization objectives namely area, power and delay are highly correlated and divergent in nature. Including variations in process parameters have made their relationship more difficult and complex to optimize. Traditional deterministic methods ignored the process variations which negatively impacts the timing yield. A pessimistic worst case consideration of variations, on the other hand can lead to severe design challenges. In this context, there is a strong need for circuit optimization methods with a statistical outlook. In this section, we designed and developed solutions for circuit optimization methods using variable thresholding technique.

A.VARIABLE THRESHOLDING TECHNIQUE

Here the circuit operates on Variable Threshold MOS logic (VTMOS). The VTMOS is based on operating the MOS devices with a suitable substrate bias which varies with gate voltage, by connecting a negative bias voltage between gate and substrate for PMOS and a positive bias voltage between gate and substrate for NMOS. With VTMOS, there will be a considerable reduction in operating current and power dissipation. Also in this design we can see that there is a significant reduction in the total number of transistors.

When we increase the bias above 0V, there is a notable change in the current-voltage characteristics and power dissipation. For VTMOS logic, there are 2 modes of operation: - ON mode and OFF mode. While considering VTNMOS, ON mode is defined as the voltage at which 

\[ V_g=1V \] and \[ V_{gs}=V_{AN} \] and OFF mode is similar to that of a normal NMOS. But for VTPMOS, when \[ V_g=0V \] and \[ V_{gs}=V_{AN} \] is defined as the ON mode and OFF mode is similar to that of a normal PMOS. The main idea behind variable thresholding scheme is to alter the threshold voltage without affecting the performance of the circuit.

Fig 3. XOR/XNOR circuit using VTMOS logic

From the circuit diagram, it is clear that the transistor count is less compared with other circuits using different optimization techniques. Due to the miniaturization in very large scale integrated (VLSI) circuits, power dissipation increases [3]. This motivates the designer to design low power circuits with less area overhead. By using variable body bias, this method involves designing a cell in which the logic can be customized. The cell is made up of variable threshold complementary metal oxide semiconductor (VTCMOS) transistors in which the body bias of both p-channel metal oxide semiconductors (PMOS) and n-channel metal oxide semiconductor (NMOS) is varied based on the logic function. By changing the body bias in VTCMOS, the leakage can be further reduced compared with conventional CMOS and the desired logic functions can be made possible.

3 ADDER AND PARITY CHECKER REALISATION USING OPTIMIZED CIRCUITS AND REVERSIBLE LOGIC

Here an attempt is made to realize 1 bit full adder using above optimized circuits. Also compared reversible and irreversible logic in terms of signal integrity.
A. REALISATION OF 1 BIT FULL ADDER USING CMOS LOGIC

A digital circuit which performs addition of numbers is called an adder. They are used in most of the arithmetic and logic units. They are also a vital component in other parts of the processor, where they are used to calculate addresses, increment and decrement operators, table indices and similar operators. Full adders are the vital components in different applications and some are digital signal processors (DSP) architectures and microprocessors. [4] The adder is one of the most critical components of a processor, as it is used in the floating-point unit, Arithmetic Logic Unit (ALU), and for address generation or for accessing memory (John Rabaei (2003). Rapid growth of mobile electronic devices such as cellular phones and laptop computers requires the use of power efficient VLSI circuits. The weak design of full adder would affect the system performance as a whole. Static or dynamic logic styles have been utilised to simulate a variety of full adders as reported in the literature. The purpose of a binary full-adder (BFA) is to implement the following truth table for each bit.

![Table 1 Truth table of 1 bit Full Adder](image)

Above truth table is realized using XOR, AND and OR gates. Here two 2 input XOR gate is required to generate SUM. CARRY is generated using 1 XOR, 2 AND and 2 OR gates. It generates a byte wide adder, if we cascade eight full adder cells together, and also propagate the carry bit from one adder to the next Logically, \( C_{out} = AB + Ci \) (A XOR B)

\[ S = A \times OR \times B \times OR \times Ci. \]

On the whole, adders of n-bits are created by chaining together these 1-bit adder slices. A transistor level implementation uses a total of 32 transistors.

B. REALISATION OF 1 BIT FULL ADDER USING OPTIMIZED CIRCUITS

Adder is implemented using transmission gate, bootstrap technique, feedback technique and VT莫斯 logic. The main advantage of using the first three configurations is such that an intermediate 2 input XOR/XNOR is generated which helps to decrease the transistor count and also helps to generate the SUM directly without cascading two XOR gates together as such as in a conventional adder. [5] Circuit realized with variable thresholding technique will have a PDP which is much lower compared with other circuits. As stated above, the PDP generated by the full-adder would crucially determine the system’s overall performance. Thus, by viewing this fact for the implementation of modern digital systems the design of a full-adder having low-power consumption and low propagation delay results of great interest.

![Fig 4. Realisation of full adder using different optimisation techniques](image)

C. PARITY CHECKER REALISATION USING IRREVERSIBLE AND REVERSIBLE LOGIC

Most of the digital systems include error detectors and signals the occurrence of errors. An error is the presence of a signal whose value is different from its desired value in a proper operating system.[6] The 2 main reasons for including error detectors in a system are to avoid the error from reaching the system output and to locate the position of error. One way of discarding error propagation is to check the received data after data transfer and, if an error is detected, either request retransmission or correct the received data using an error correcting code (as in RAMS). Another way is repeat the operation if the result if the system detects any error [8]. Almost all large systems typically include error detectors, along with circuitry to record the location and frequency of error events. This information is used to facilitate accuracy and fast maintenance.

A major issue in present day technology is energy dissipation. In high technology circuits and systems, energy is dissipated due to information loss which is constructed using irreversible hardware. The loss of one bit of information will dissipate \( kT \ln (2) \) joules of energy as stated by Landauer’s principle, where, \( k \) is the Boltzmann’s constant and \( k=1.38x10^{-23} \) J/K, \( T \) is the absolute temperature in Kelvin. [7] For every bit of information, the primitive combinational logic circuits dissipate heat energy that is lost during the operation. This is based on the second law of thermodynamics i.e., once the information is lost, it cannot be recovered by any methods.
4. SIMULATION RESULTS

Table 2 Truth table for irreversible XOR logic

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

In 1973, Bennett showed the relevance of reversible circuits in order to avoid kTln2 joules of energy dissipation in a circuit. In this paper we have compared reversible and irreversible logic. Reversible circuits are those circuits which do not lose energy during operation. [9] For parity checking, irreversible logic requires an additional parity bit to ensure signal integrity. But in case of reversible logic, no such additional bit is needed.

Table 3 Truth table for reversible logic

<table>
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<th>Inputs</th>
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</tr>
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<td>A</td>
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</table>

For parity checking, irreversible logic requires an additional parity bit to ensure signal integrity. But in case of reversible logic, no such additional bit is needed.

Fig 5. Realisation of parity checker using reversible logic

Fig 6. Simulation result of XOR/XNOR circuit using VTMOS logic

Fig 7. Parity Checker realisation using irreversible and reversible logic

All simulations are carried out in HSPICE 130nm CMOS technology. Different optimization and correction techniques like transmission gates, feedback technique, bootstrap technique and variable thresholding is used to ensure the design a reliable overall performance. The main motivation for using these technique is to decrease power consumption, delay and area[10].

Table 4 Comparison of Basic XOR/XNOR circuits and VTMOS logic

<table>
<thead>
<tr>
<th>CIRCUITS</th>
<th>NUMBER OF TRANSISTORS</th>
<th>POWER (nW)</th>
<th>DELAY (ns)</th>
<th>PDF (pA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BASIC XOR/XNOR</td>
<td>32</td>
<td>3.846</td>
<td>3.012</td>
<td>1.067</td>
</tr>
<tr>
<td>VTMOS LOGIC</td>
<td>14</td>
<td>1.685</td>
<td>3.00</td>
<td>0.565</td>
</tr>
</tbody>
</table>
4 CONCLUSION

In this work, a new high performance three-input XOR/XNOR circuit with less PDP and occupied area are conceived using systematic cell design methodology.[11] This well organised design methodology is used to make the design energy and area efficient. The new circuit enjoys higher transistor density, noise immunity and driving capability with low-voltage operation, and the least probability to produce glitches. On average, the circuit with VT莫斯 logic exhibits 31.30% improvement in delay. [12] Since XOR circuits are relevant in adders and parity checker circuits, adder using VT莫斯 logic and parity checker using reversible logic is designed and analysed in HSPICE simulation based on the TSMC 0.13-μm technology. The simulation results demonstrates that VT莫斯 adder circuit exhibits 51.31% improvement in delay and reversible parity checker circuit possesses 49.8% decreased delay and 48.3% improvement in PDP. Simulation results depicts that the proposed circuits exhibit better performances compared to previously suggested circuits.

REFERENCES